## ABSTRACT

A microprocessor chip with an instruction processor designed to execute instructions of first and second instruction sets. A memory for use with the chip is divided into pages for management by a virtual memory manager. Instructions are stored in different memory pages of a single address space, and are coded for computers of two different instruction sets, and use two different calling conventions. A table has entries corresponding to pages of the memory. A switch in the chip is responsive to a first flag value stored in each table entry, and controls the instruction processor to interpret instructions under, alternately, the first or second instruction set as directed by the first flag value of the table entry corresponding to an instruction's memory page. The chip recognizes when program execution has transferred from a page of instructions using the first data storage convention to a page of instructions using the second data storage convention, as indicated by second flag values stored in table entries corresponding to the respective pages, and in response to the recognition, to adjust a data storage content of the computer from the first storage convention to the second data storage convention. The history record is designed to provide to the manager a record of a classification of a recently-executed instruction. A caller can call two callee subprograms, each of the two subprograms being coded in two different instruction sets; the caller need not be aware of the instruction set difference, nor prepare differently to call the two callees.